WHAT IS CLAIMED IS:

1. A code division multiple access (CDMA) integrated circuit, comprising:

a demodulator configured to correlate an input data with a plurality of codes; and

a test data pattern generator configured to spread an input test data with at least one of the plurality of codes to form a spread test data, and to provide the spread test data to the demodulator.

2. The integrated circuit of claim 1 further comprising a multiplexer configured to multiplex the input data and the spread test data to the demodulator.

3. The integrated circuit of claim 1 wherein at least one of the plurality of codes comprises a scrambling code and a spreading code.

4. The integrated circuit of claim 3 wherein the scrambling code comprises a pseudo-random noise (PN) code and the spreading code comprises a Walsh code.

5. The integrated circuit of claim 3 wherein the test pattern generator further comprises a plurality of AND gates configured to gate off the scrambling code.

6. The integrated circuit of claim 3 wherein the test pattern generator further comprises a plurality of AND gates configured to gate off the spreading code.

7. The integrated circuit of claim 1 wherein the test data pattern generator further comprises a combiner configured to combine a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes.

8. The integrated circuit of claim 7 wherein the combiner comprises a logical XOR circuit.

9. The integrated circuit of claim 7 wherein the test data pattern generator further comprises a multiplexer configured to select the scrambling code from a plurality of scrambling codes, select the spreading code from a plurality of spreading codes, and provide the scrambling code and spreading code to the combiner.

10. The integrated circuit of claim 9 wherein the demodulator further comprises a rake receiver having a plurality of fingers, one of the fingers being configured to receive the scrambling code and the spreading code.

11. The integrated circuit of claim 1 wherein the test data pattern generator further comprises a plurality of spreaders configured to spread the input test data with the plurality of codes to form a plurality of spread test data

12. The integrated circuit of claim 11 wherein the test data pattern generator further comprises a plurality of AND gates configured to gate off at least one spread test data.

13. A code division multiple access (CDMA) integrated circuit, comprising:
means to correlate an input data with a plurality of codes; and
means to spread an input test data with at least one of the plurality of codes to form a spread test data, and to provide the spread test data as the input data.

14. The integrated circuit of claim 13 further comprising means to multiplex the input data and the spread test data.

15. The integrated circuit of claim 13 wherein at least one of the plurality of codes comprises a scrambling code and a spreading code.

16. The integrated circuit of claim 15 wherein the scrambling code comprises a pseudo-random noise (PN) code and the spreading code comprises a Walsh code.

17. The integrated circuit of claim 15 further comprises means to gate off the scrambling code and means to gate off the spreading code.

18. The integrated circuit of claim 13 further comprises means to combine a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes.

19. The integrated circuit of claim 18 further comprises means to select the scrambling code from a plurality of scrambling codes and to select the spreading code from a plurality of spreading codes.

20. A method of testing a code division multiple access (CDMA) integrated circuit, comprising the steps of:

correlating an input data with a plurality of codes within a demodulator; and

spreading an input test data with at least one of the plurality of codes to form a spread test data, and providing the spread test data to the demodulator.

21. The method of claim 20 further comprising the step of multiplexing the input data and the spread test data.

22. The method of claim 20 wherein at least one of the plurality of codes comprises a scrambling code and a spreading code.

23. The method of claim 20 further comprises the step of combining a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes.